VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the claims as follows:

1. (AMENDED) A programmable logic device comprising:

one or more horizontal routing channels;

one or more vertical routing channels;

one or more logic elements each configured to connect between one of said horizontal routing channels and one of said vertical routing channels, wherein each of said logic [element] elements comprises (i) a logic block array, and (ii) an interconnect matrix coupled to said logic block array, said horizontal routing channel and said vertical routing channel; and

a memory block coupled to either (a) said interconnect matrix or (b) said horizontal routing channel and said vertical routing channel.

2. (AMENDED) The programmable logic device according to claim 1, wherein said memory block comprises a first port [is] connected to one of said horizontal routing channels and a second port connected to one of said vertical routing channels.

6. (AMENDED) The programmable logic device of claim 1, wherein said memory block is [placed within said logic block array] coupled to said interconnect matrix.

17. (ADDED) The programmable logic device of claim 1, wherein said logic block array comprises a plurality of logic blocks.

18. (ADDED) The programmable logic device of claim 17, wherein each logic block of said logic block array comprises a product term array configured to receive inputs from said interconnect matrix.

19. (ADDED) The programmable logic device of claim 18, wherein each of said logic blocks further comprise a plurality of macrocells each having an output coupled to said interconnect matrix.

20. (ADDED) The programmable logic device of claim 19, wherein each of said logic blocks further comprises an OR array coupling said product term array to said plurality of macrocells.

21. (ADDED) The programmable logic device of claim 1, wherein said interconnect matrix comprises a programmable interconnect matrix.

22. (ADDED) The programmable logic device of claim 6, wherein said interconnect matrix couples said memory block to one

of said horizontal routing channels, one of said vertical routing channels, and said logic block array.

23. (ADDED) The programmable logic device of claim 1, comprising a plurality of horizontal routing channels and a plurality of vertical routing channels.

24. (ADDED) The programmable logic device of claim 1, comprising a plurality of logic elements.

25. (ADDED) The programmable logic device of claim 23, comprising at least four logic elements.

26. (ADDED) A programmable logic device comprising:

a plurality of horizontal routing channels;

a plurality of vertical routing channels;

a plurality of first memory blocks; and

a plurality of logic block arrays, wherein each of said plurality of first memory blocks and each of said plurality of logic block arrays is coupled between one of said plurality of horizontal routing channels and one of said plurality of vertical routing channels.

27. (ADDED) The programmable logic device according to claim 26, wherein each of said first memory blocks comprises a first port connected to one of said horizontal routing channels and a second port connected to one of said vertical routing channels.

28. (ADDED) The programmable logic device according to claim 26, wherein each of said first memory blocks is configurable to a mode selected from the group consisting of (i) an asynchronous dual port memory mode, (ii) a synchronous dual port memory mode, and (iii) a synchronous FIFO memory mode.

29. (ADDED) The programmable logic device of claim 26, wherein each of said logic block arrays comprises a plurality of programmably interconnected logic blocks, and each of said logic blocks comprises a plurality of macrocells.

30. (ADDED) The programmable logic device of claim 26, comprising:

M number of horizontal routing channels;

N number of vertical routing channels;

N times M number of first memory blocks; and

N times M number of logic block arrays, wherein N plus M is greater than or equal to 2.

31. (ADDED) The programmable logic device of claim 26, wherein each of said logic block arrays further comprises an interconnect matrix coupled to said horizontal routing channel and said vertical routing channel.

32. (ADDED) The programmable logic device of claim 31, wherein each of said logic block arrays further comprises a second memory block coupled to said interconnect matrix.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a programmable logic device comprising one or more horizontal routing channels, one or more vertical routing channels, one or more logic elements, and a memory block. Each of the one or more logic elements may be configured to connect between one of said horizontal routing channels and one of said vertical routing channels. The logic elements may comprise (i) a logic block array and (ii) an interconnect matrix coupled to the logic block array, the horizontal routing channel and the vertical routing channel. The memory block may be coupled to either the interconnect matrix or the horizontal routing channel and the vertical routing channel.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims may be found in the drawings (e.g., FIGS. 2, 3, and 8) and the specification (e.g., page 4, lines 17-18, page 10, line 19 through page 12, line 8 and page 20, line 1 through page 22, line 21), as originally filed. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 6, 7, and 10-15 under 35 U.S.C. §102(b) as being anticipated by Cliff et al. ('195) has been obviated by appropriate amendment and should be withdrawn.

Cliff et al. disclose a programmable logic array integrated circuit device (Title). The programmable logic array integrated circuit device includes a plurality of regions 20 of programmable logic disposed in a two-dimensional array of intersecting rows and columns (Abstract and FIG. 1 of Cliff). Interconnection conductors are associated with each row and column (Abstract). The interconnection conductors of Cliff associated with each row include conductors 60 that extend continuously along the entire length of the row and conductors 70 that extend continuously along only the left or right half of the row (Abstract and FIG. 1 of Cliff). The device of Cliff includes a central column of random access memory regions 40 (column 5, lines 25-32 of Cliff). One RAM region 40 is associated with each row of the device (column 13, lines 40-41 of Cliff). Each of the regions 20 includes a plurality of subregions or logic modules 30 (column 5, lines 33-34). Logic signals are fed to each of the logic modules 30 in a region 20 using region feeding conductors 90. The region feeding conductors 90 bring signals to the logic modules 30 from **only** the horizontal conductors 60 and 70 (FIG. 3 of Cliff). Cliff

et al. appear to be silent regarding the region feeding conductors 90 connecting the logic modules 30 to the vertical conductors 80.

In contrast, the presently claimed invention provides a logic element comprising (i) a logic block array and (ii) an interconnect matrix coupled to the logic block array, a horizontal routing channel **and** a vertical routing channel. Assuming, *arguendo*, that (i) the presently claimed horizontal routing channel is similar to the horizontal interconnection conductors 60 and 70 of Cliff, (ii) the vertical routing channels are similar to the vertical interconnection conductors 80 of Cliff and (iii) the logic block array is similar to the plurality of logic modules 30 of Cliff (for which Applicants' representative does not necessarily agree), Cliff et al. do not appear to disclose or suggest all of the elements of the presently claimed invention.

Specifically, Cliff et al. disclose that the plurality of logic modules 30 are connected to each other and to the horizontal interconnection conductors 60 and 70 via the region feeding conductors 90 (FIG. 3 of Cliff and column 9, lines 7-40). The region feeding conductors 90 do not appear to connect the logic modules 30 to the vertical interconnection conductors 80 (see FIG. 3 of Cliff). Therefore, Cliff et al. do not disclose or suggest an interconnect matrix coupled to the logic block array, the horizontal routing channel **and** the vertical routing channel, as is presently claimed. As such, Cliff et al. do not disclose or

suggest all of the elements of the presently claimed invention and the rejection should be withdrawn.

In addition, new independent claim 26 is believed to be fully patentable over Cliff et al. Claim 26 provides a plurality of first memory blocks and a plurality of logic block arrays where each of the plurality of first memory blocks and each of the plurality of logic block arrays is coupled between one of a plurality of horizontal routing channels and one of a plurality of vertical routing channels. Assuming, *arguendo*, that (i) the presently claimed horizontal routing channel is similar to the horizontal interconnection conductors 60 and 70 of Cliff, (ii) the vertical routing channels are similar to the vertical interconnection conductors 80 of Cliff, (iii) the logic block array is similar to the plurality of logic modules 30 of Cliff and (iv) the first memory block is similar to the RAM regions 40 of Cliff (for which Applicants' representative does not necessarily agree), Cliff et al. do not appear to disclose or suggest all of the elements of the presently claimed invention.

Specifically, Cliff et al. disclose that the plurality of logic modules 30 are connected to each other and to the horizontal interconnection conductors 60 and 70 via the region feeding conductors 90 (FIG. 3 of Cliff and column 9, lines 7-40). The region feeding conductors 90 do not appear to connect the logic modules 30 to the vertical interconnection conductors 80 (see FIG.

3 of Cliff). In addition, the RAM regions 40 do not appear to connect to the vertical interconnection conductors 80, but rather, are connected to separate vertical interconnection conductors 80' that extend along the column of RAM regions (FIGS 1, 2, and 7 and column 8, lines 1-10 of Cliff). Therefore, Cliff et al. do not disclose or suggest a plurality of first memory blocks and a plurality of logic block arrays where each of the plurality of first memory blocks **and** each of the plurality of logic block arrays is coupled between one of the plurality of horizontal routing channels **and** one of the plurality of vertical routing channels, as is presently claimed. As such, Cliff et al. do not disclose or suggest all of the elements of claim 26 and, therefore, the presently claimed invention is fully patentable over the cited reference.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejections of claims 3-4 under 35 U.S.C. §103 as being unpatentable over Cliff et al. in view of Veenstra and claims 12 and 16 under 35 U.S.C. §103 as being unpatentable over Cliff et al in view of Jefferson et al. have been obviated by appropriate amendment and should be withdrawn.

Claims 3, 4, 12, and 16 depend either directly or indirectly from independent claim 1, which for the reasons stated above is believed to be fully patentable over Cliff et al.

Veenstra and Jefferson et al., alone or in combination do not cure the deficiencies of Cliff et al.

Veenstra discloses an embedded memory block with a FIFO mode for a programmable logic device (Title). A logic array block 220 of Veenstra and an embedded array block 240 of Veenstra appear to connect to different sets of vertical conductors 264 of Veenstra (FIG. 2 and column 4, lines 22-44).

In contrast, the presently claimed invention provides (a) a logic element comprising (i) a logic block array and (ii) an interconnect matrix coupled to the logic block array, a horizontal routing channel **and** a vertical routing channel and (b) a memory block coupled to either the interconnect matrix or the horizontal routing channel and the vertical routing channel. Assuming, *arguendo*, that (i) the presently claimed horizontal routing channel is similar to the horizontal conductors 262 of Jefferson, (ii) the vertical routing channels are similar to the vertical conductors 264 of Jefferson, (iii) the logic block array is similar to the logic array block 220 of Jefferson and (iv) the first memory block is similar to the embedded array block 240 of Jefferson (for which Applicants' representative does not necessarily agree), Jefferson et al. do not appear to disclose or suggest all of the elements of the presently claimed invention.

Specifically, since the logic array block 220 of Veenstra and the embedded array block 240 of Veenstra are connected to

different sets of vertical conductors, Veenstra does not teach or suggest a logic element comprising (i) a logic block array and (ii) an interconnect matrix coupled to the logic block array, a horizontal routing channel and a vertical routing channel and (b) a memory block coupled to either the interconnect matrix or the horizontal routing channel and the vertical routing channel, as presently claimed. Therefore, Veenstra does not teach or suggest all the elements of the presently claimed invention.

Jefferson et al. do not cure the deficiencies of Cliff et al. and/or Veenstra. Jefferson et al. disclose a programmable logic integrated circuit with an on chip DLL or PLL for clock distribution (Title). Jefferson et al. appear to be silent regarding a memory block coupled to either the interconnect matrix or the horizontal routing channel and the vertical routing channel, as is presently claimed. Since Jefferson et al. are silent regarding a memory block coupled to either the interconnect matrix or the horizontal routing channel and the vertical routing channel, Jefferson et al. do not teach or suggest a logic element comprising (i) a logic block array and (ii) an interconnect matrix coupled to the logic block array, a horizontal routing channel and a vertical routing channel and (b) a memory block coupled to either the interconnect matrix or the horizontal routing channel and the vertical routing channel, as presently claimed. Therefore,

Jefferson et al. do not teach or suggest all the elements of the presently claimed invention.

Cliff et al., Veenstra, and Jefferson et al., either alone or in combination, do not teach or suggest all the elements of the presently claimed invention. As such, the presently claimed invention is believed to be fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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